CLAIMS

What is claimed is:

1. A method comprising:

receiving a packet at a network device;

pre-fetching a protocol control block (PCB) associated with the packet into a cache;

queuing the packet for processing; and

retrieving the PCB from the cache when a processing unit is ready to process the packet.

2. The method of claim 1, further comprising pre-fetching a header associated with the packet into the cache.

3. The method of claim 2, further comprising retrieving the packet header from the cache when the processing unit is ready to process the packet.

4. The method of claim 1, further comprising sending an interrupt to notify the processing unit of the receipt of the packet.

5. The method of claim 1, wherein pre-fetching a PCB associated with the packet into a cache comprises pre-fetching a PCB associated with the packet into a cache of the processing unit.

6. The method of claim 5, further comprising storing the packet in a memory coupled to the processing unit.

7. The method of claim 1, further comprising processing the packet.

8. An apparatus comprising:

a receive unit to receive a packet;

a pre-fetch unit coupled to the receive unit to pre-fetch a protocol control block (PCB) associated with the packet into a cache and queue the packet for processing; and

a processing unit coupled to the pre-fetch unit to retrieve the PCB from the cache and process the packet.

9. The apparatus of claim 8, wherein the receive unit is a network interface card.

10. The apparatus of claim 8, wherein the pre-fetch unit to further pre-fetch a header associated with the packet into the cache.

11. The apparatus of claim 10, wherein the processing unit to further retrieve the packet header from the cache.

12. The apparatus of claim 8, wherein the pre-fetch unit to pre-fetch a PCB associated with the packet into a cache comprises the pre-fetch unit to pre-fetch a PCB associated with the packet into a cache of the processing unit.

13. The apparatus of claim 8, further comprising an interrupt unit coupled to the receive unit and the processing unit to receive an interrupt from the receive unit and notify the processing unit of the packet.

14. An article of manufacture comprising:

a machine accessible medium including content that when accessed by a machine causes the machine to:

receive a packet;

pre-fetch a protocol control block (PCB) associated with the packet into a cache;

queue the packet for processing; and

retrieve the PCB from the cache when a processing unit is ready to process the packet.

15. The article of manufacture of claim 14, wherein the machine-accessible medium further includes content that causes the machine to pre-fetch a header associated with the packet into the cache.

16. The article of manufacture of claim 15, wherein the machine-accessible medium further includes content that causes the machine to retrieve the packet header from the cache when the processing unit is ready to process the packet.

17. The article of manufacture of claim 14, wherein the machine-accessible medium further includes content that causes the machine to process the packet.

18. The article of manufacture of claim 14, wherein the machine-accessible medium further includes content that causes the machine to send an interrupt to notify the processing unit of the receipt of the packet.

19. The article of manufacture of claim 14, wherein the machine accessible medium including content that when accessed by the machine causes the machine to pre-fetch a PCB associated with the packet into a cache comprises the machine

accessible medium including content that when accessed by the machine causes the machine to pre-fetch a PCB associated with the packet into a cache of the processing unit.

20. The article of manufacture of claim 14, wherein the machine-accessible medium further includes content that causes the machine to store the packet in a memory coupled to the processing unit.

21. A system comprising:

a receive unit to receive a packet;

a memory coupled to the receive unit to store the received packet;

a memory controller coupled to the memory to manage the memory;

a pre-fetch unit coupled to the receive unit to pre-fetch a protocol control block (PCB) associated with the packet into a cache and queue the packet for processing; and

a processing unit to retrieve the PCB from the cache and process the packet.

22. The system of claim 21, wherein the receive unit is a network interface card.

23. The system of claim 21, wherein the pre-fetch unit to further pre-fetch a header associated with the packet into the cache.

24. The system of claim 23, wherein the processing unit to further retrieve the packet header from the cache.

25. The system of claim 21, further comprising an interrupt unit coupled to the receive unit and the processing unit to receive an interrupt from the receive unit and notify the processing unit of the packet.